Audio Codec ‘97

Component Specification

Revision 1.03

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Primary developers:

Analog Devices
Creative Labs
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Yamaha Corporation

REVISION HISTORY

1.00	AC '97 Component Specification revision 1.0, released May 17, 1996
1.01	**Page 32, 6.3:** duplicate 6.3 heading moved and renamed 6.1.1 (no text changed) **Page 34, 6.3.1, para 2, line 3:** ~~the~~ each vendors... **Page 39, 6.3.11, para 1, line 4:** ~~bits~~ bits 0-7.
1.02	AC '97 Component Specification revision 1.02, posted on the Web June 1, 1996
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1.03	AC '97 Component Specification revision 1.03, updated September 22, 1996
	Page 7, 1.1, Feature List, bullet 2: Two standard packages: 48-pins ~~package, alternate~~ and 64-pins ~~package~~
	Page 11, 2., Packaging, para 2: ...48-pin package is attractive ~~a requirement~~ for migrating *baseline motherboard*...
	Page 11, 2., Packaging, para 3: The standard ~~alternate~~ 64-pin package...
	Page 15, 2.2, Table 2: 64-pin package **"**Reserved" pins 41-44 assigned as generic caps or multi-channel outputs
	Page 18, 3.3, Table 5, 1st entry: Vref ~~Vref1~~
	Page 18, 3.3, Table 5: added references to CAP2, CAP11-CAP13, CAP25-CAP28
	Page 19, 3.3, bullets: added references to CAP25-CAP28
	Page 29, 5.2, para 1: ...When AC '97's ~~General Purpose Register (20h),~~ Powerdown Register (26h), is...
	Page 29, 5.2, para 2: ...the write to the ~~General Purpose Register (20h)~~ Powerdown Register (26h) with PR4.
	Page 33, 6.3, Table 7: PC_BEEP Default x000h can be 0000h or 8000h (mute off or on)
	Page 33, 6.3, Table 7: Phone Volume (0Ch) and Mic Volume (0Eh) register D5 bits: were *GN5*, now X (don't care)
	Page 36, 6.3.4, PC Beep, para 2: Inserted new 2nd paragraph and reference to AC '97 FAQ for further details.
	Page 36, 6.3.4, PC Beep, para 3: Note**:** The PC Beep is recommended ~~required~~ to be routed to...
	Page 36, 6.3.4, PC Beep, para 4: The default value can be 0000h or 8000h...mute off or on
	Page 38, 6.3.9, 3D Control Register: linear or logarithmic implementation is acceptable (linear is shown)
	Page 41, 7., para 1: ...by the ~~General Purpose Register (index 20h)~~ Powerdown Register (26h).
	Page 41, 7., para 2: ...writes to the ~~General Purpose~~ Powerdown Register are performed...
	Page 43, 9.1., parenthesis: ($T_{ambient}$ = 25^{0}C, AVdd = DVdd = 5.0 V or 3.3V **+/- 5%;** ...
	Page 43, 9.1., NOTE: ... either 5.0V or 3.3V **(+/- 5%),** ...
	Page 43, 9.1., para 2: added 2nd paragraph and 2 tables specifying PCI 2.1 compliant 5.0 V and 3.3 V operation
	Page 46, 9.2.3., figure: shows setup and hold times for SYNC, SDATA_OUT, and SDATA_IN (at Controller)
	Page 46, 9.2.4., table: added 6nS spec for Max rise and fall times (for all entries in table)
	Page 48, 10., parenthesis: ... $T_{ambient}$ = 25^{0}C, AVdd = DVdd = 5.0 V **+/- 5%;** ... tone and 3D disabled).
	Page 48, 10., Table: Vrefout spec'd at 2.25 - 2.75 V typical
	Page 48, 10., Note 7: added clarification of Stop Band rejection
	Page 48, 10., Note 8: added clarification of Out-of-Band rejection

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. Introduction

1.1. Feature List

- Analog I/O component of 2-chip PC audio solution
- Two standard packages: 48-pins and 64-pins
- Split digital/analog architecture for improved S/N ratio (> 90dB achievable)
- 16-bit stereo full-duplex Codec with fixed 48K sampling rate
- Four analog line-level stereo inputs for connection from LINE IN, CD, VIDEO and AUX
- Two analog line-level mono inputs for speakerphone (or DLP[1]) and PC BEEP
- Mono mic input switchable from two external sources
- High quality pseudo-differential CD input
- Stereo line level output
- Mono output for speakerphone (or DLP[1])
- Power management support
- Optional tone control
- Optional loudness control
- Optional 3D stereo enhancement
- Optional stereo headphone output with 32 Ohm drive
- Optional 18 or 20-bit DAC and ADC resolution
- Optional modem line Codec (ADC and DAC)
- Optional 3rd ADC input channel for mic

[1] Down Line Phone

1.2. Audio Codec ‘97 Architectural Overview

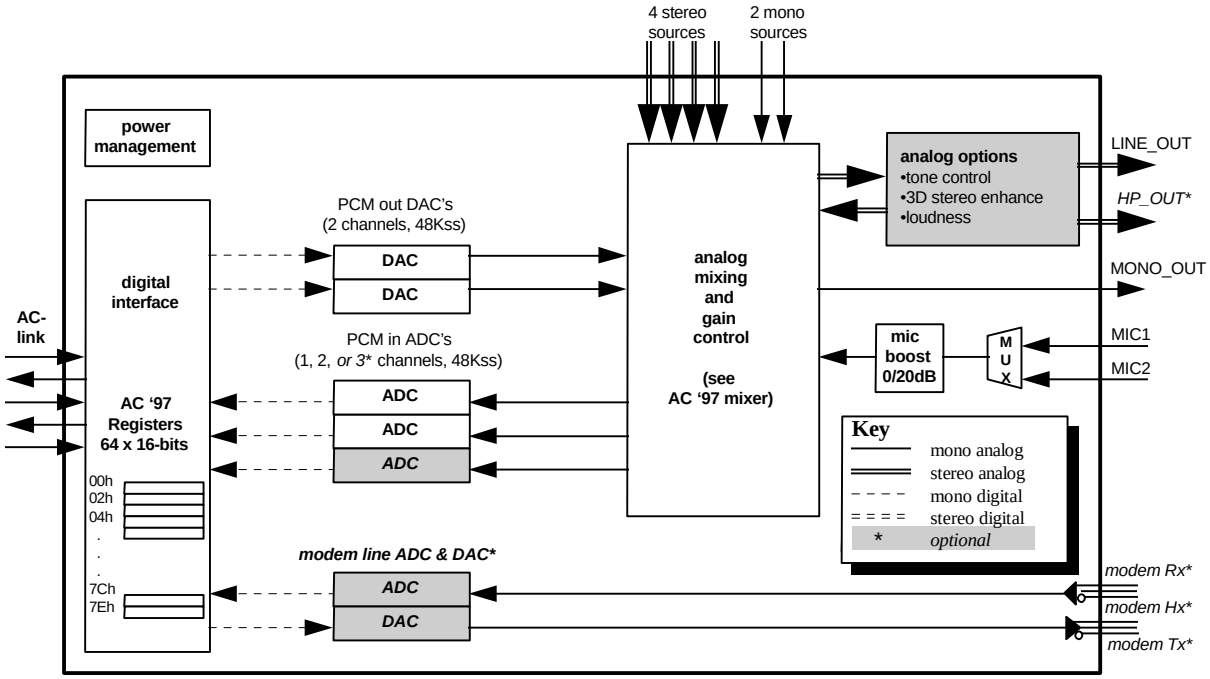


Figure 1. AC ‘97 Block Diagram

Figure 1 shows the functional blocks that make up the Audio Codec ‘97, which is the analog component of a 2-chip audio solution (fully described in the next section). The two fixed 48Kss DAC’s support a stereo PCM out channel which contains a mix generated in the AC ‘97 controller of all software sources, including the internal synthesizer and any other digital sources. PCM out is mixed with additional analog sources, processed with optional 3D stereo enhancement and tone controls, and sent to independently controlled LINE_OUT and HP_OUT. For speakerphone telephony, the MONO_OUT delivers either mic only or a mono mix of sources to the telephony subsystem.

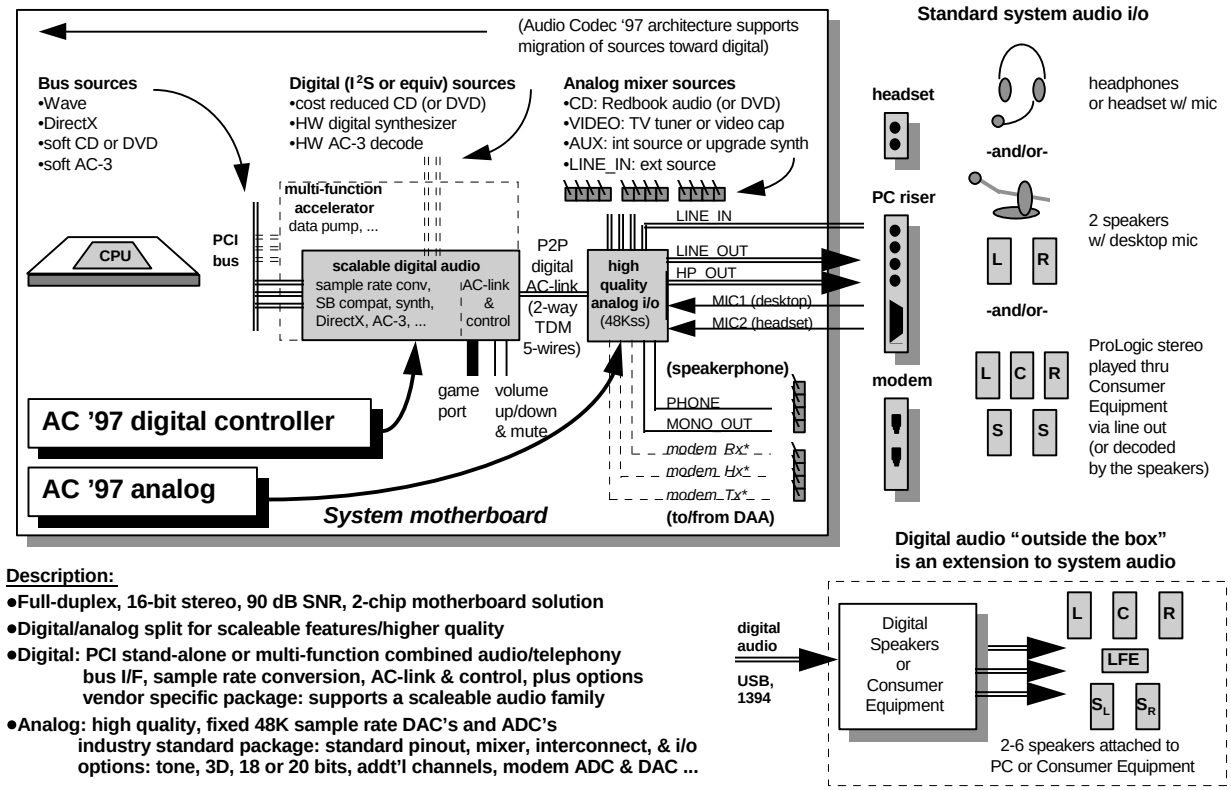
The ADC path supports 2 channels of fixed 48Kss input, with an option to support a 3rd fixed 48Kss ADC input channel dedicated to the mic. The standard stereo PCM in channel supports record of any mono or stereo source, or a mix of sources[2]. The optional dedicated mic channel extends the range of acoustic echo cancellation capabilities by allowing the audio subsystem to record the MIC along with LINE_OUT (L and R) reference signals needed for robust stereo mic input filtering, either in the AC ‘97 controller or on the host CPU. The independent mic channel also has the potential to be dedicated to voice input applications.

The optional ADC and DAC pair supports integration of the line Codec portion of a modem AFE function into AC ‘97.

NAMING CONVENTION: Throughout this document signal names have been assigned to be consistent with the point of view of an application running on the PC.

[2] For highest quality and greatest flexibility, the AC ‘97 controller should provide the capability to ***digitally*** record any or all of the contributing digital sources in the PCM out mix.

1.3. Integrating AC ‘97 into the System



Description:

- **Full-duplex, 16-bit stereo, 90 dB SNR, 2-chip motherboard solution**
- **Digital/analog split for scaleable features/higher quality**
- **Digital: PCI stand-alone or multi-function combined audio/telephony bus I/F, sample rate conversion, AC-link & control, plus options vendor specific package: supports a scaleable audio family**
- **Analog: high quality, fixed 48K sample rate DAC’s and ADC’s industry standard package: standard pinout, mixer, interconnect, & i/o options: tone, 3D, 18 or 20 bits, addt’l channels, modem ADC & DAC ...**

Figure 2. AC ‘97 System Diagram

The System Diagram in Figure 2 shows the essential features of an AC ‘97 audio design. The AC ‘97 analog component performs fixed 48K sample rate DAC & ADC conversions, mixing, and analog processing (tone, 3D stereo enhancement, etc.). It always functions as a slave to an AC ‘97 digital controller which must be implemented in the digital portion of any AC ‘97 audio system.

The AC ’97 controller, primarily targeted for PCI, can be as simple as a stand-alone design which supports high quality sample rate conversions to/from 48Kss, Sound Blaster* compatibility, FM and/or wavetable synthesis, with optional DirectSound* acceleration, AC-3 decode, etc. The AC ’97 controller may also be embedded within a PCI multifunction accelerator, offering higher levels of integration by combining audio with telephony or graphics. However, nothing precludes ISA, USB, or 1394 designs based on the AC ’97 architecture.

The digital link, "AC-link", connecting the AC `97 controller to the AC `97 analog is a bi-directional, 5-wire, serial TDM format interface, designed for dedicated point to point interconnect on a circuit board.

The diagram shows the most common (high attach rate) connections, some digital and some analog. PC audio today requires that a number of analog sources be supported in the analog mixer. Over time, it will become attractive from both cost and functionality perspectives to move these sources toward dedicated digital connections or onto the bus[3]. The AC ‘97 architecture facilitates this migration.

[3] The support for dedicated digital connections requires frequency locking and sample rate conversion capabilities in the AC ’97 controller in order to reconcile independent time bases, the digital source and AC ‘97’s fixed 48Kss.

The AC ‘97 architecture is designed primarily to support stereo 2-speaker PC audio. However, two multi-channel extensions are shown in the system diagram, one utilizing the AC ‘97 architecture and one independent of it:

- Multi-channel encoded stereo (such as Dolby* ProLogic*) can be played out through the 2-channel AC ’97 audio subsystem. This type of signal can be played on normal stereo speakers, decoded into 4 channels by the speakers, or sent to consumer equipment via a stereo analog line out connection.
- True 2/4/6 channel digital audio output (such as 5.1 channel Dolby AC-3*) can bypass the 2-channel AC ‘97 audio subsystem and be transmitted via a digital link (such as USB or 1394) to digital speakers or digital ready consumer equipment which drives a multi-speaker arrangement such as the home theater[4].

1.4. Software Driver support and AC ’97 controller / AC ‘97 Interoperability

Regardless of the bus and level of integration chosen, the driver written for the AC ‘97 controller is responsible for exposing and managing the AC ‘97 analog features. Interoperability requires that every AC ‘97 controller and AC ‘97 driver support the basic AC ‘97 features.

Every AC ’97 controller must be capable of performing high quality (90dB SNR) sample rate conversions on a minimum of 4 simultaneous channels (stereo out + stereo in), between a variety of sample rates and 48Kss:

- 8.0, 11.025, 16.0, 22.05, 32.0, 44.1Kss

Mono PCM output always translates in the AC ’97 controller to 2 mono channels (L and R) on the AC-link.

The following optional AC ‘97 features should also be supported by all AC ’97 controller drivers when determined to be present:

- tone control
- loudness
- simulated stereo
- 3D stereo enhancement
- headphone out

Other features may not make sense to support unless there is also support in the AC ‘97 controller. In these cases interoperability may be limited to an AC ’97 controller / AC ‘97 analog pair sourced by the same vendor:

- Modem ADC and DAC
- 3rd ADC input channel
- Vendor specific features

[4] There are many PC audio sources which are not currently bus independent, such as DOS games, HW accelerated Windows* 95 games, CD Redbook audio, and DVD-ROM movies w/ HW AC-3 decode. In order to hear ALL PC audio sources through one set of digitally connected speakers, backwards compatability must be addressed.

2. Packaging

The AC ‘97 component is available in two industry standard QFP packages, a 7mm x 7mm body 48-pin package, and a 10mm x 10mm body 64-pin package. Both packages offer SQFP and TQFP versions.

The standard 48-pin package offers OEM’s a very attractive motherboard footprint (9x9=81sq mm including pads) but may force the AC ‘97 vendor to make implementation tradeoffs between optional features, fabrication process, die size capacity, and available pins. The AC ‘97 Working Group believes that the 48-pin package is a attractive for migrating *baseline motherboard audio* to the high quality 2-chip PCI audio solution in 1997.

The standard 64-pin package offers both OEM’s and the AC ‘97 vendor the potential for higher levels of integration and more optional features, but increases the footprint (12x12=144sq mm including pads). The benefits of the 64-pin package are increased die size capacity, and 16 additional pins which support dedicated features, an additional analog power and ground, and reserved headroom for future expansion. The AC ‘97 Working Group believes that the 64-pin package is attractive for *highly integrated motherboard* PCI solutions which combine audio with telephony, and ideal for *high performance add-in cards*, as well as *external “digital audio”* solutions on USB or 1394.

Due to the fact that AC ‘97 components will be supplied by more than one vendor, there may be minor variations across the variety of 48-pin and 64-pin package options. The Intel members of AC ‘97 Working Group will provide an AC ’97 system design guide in 2H96 which will include a universal land pattern (pad layout) for both package options. The intent is to provide a single pad layout that will accommodate all available variants of the 48 and 64-pin packages.

2.1 48-pin QFP package

The pinout for the 48-pin package is shown in Figure 3, the package mechanicals are shown in Figure 4, and the pinlist is given in Table 1.

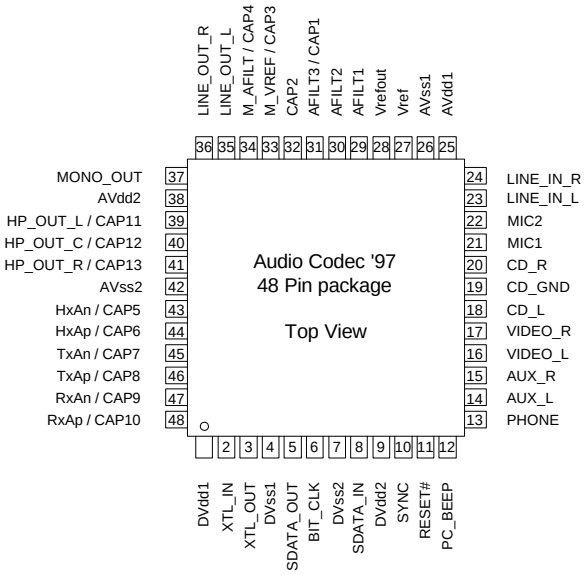
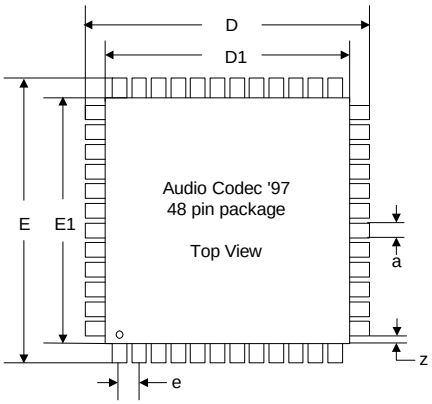


Figure 3. AC ‘97 48-pin package and pinout



Key	Dimension
D	9.00 mm
D1	7.00 mm
E	9.00 mm
E1	7.00 mm
a (lead width)	0.20 mm
e (pitch)	0.50 mm
z	1.00 mm

Figure 4. AC ‘97 48-pin package dimensions

Pin #	Signal Name	Pin#	Signal Name
1	DVdd1	25	AVdd1
2	XTL_IN	26	AVss1
3	XTL_OUT	27	Vref
4	DVss1	28	Vrefout
5	SDATA_OUT	29	AFILT1
6	BIT_CLK	30	AFILT2
7	DVss2	31	AFILT3 / CAP1
8	SDATA_IN	32	CAP2
9	DVdd2	33	M_VREF / CAP3
10	SYNC	34	M_AFILT / CAP4
11	RESET#	35	LINE_OUT_L
12	PC_BEEP	36	LINE_OUT_R
13	PHONE	37	MONO_OUT
14	AUX_L	38	AVdd2
15	AUX_R	39	HP_OUT_L / CAP11
16	VIDEO_L	40	HP_OUT_C / CAP12
17	VIDEO_R	41	HP_OUT_R / CAP13
18	CD_L	42	AVss2
19	CD_GND	43	HxAn / CAP5
20	CD_R	44	HxAp / CAP6
21	MIC1	45	TxAn / CAP7
22	MIC2	46	TxAp / CAP8
23	LINE_IN_L	47	RxAn / CAP9
24	LINE_IN_R	48	RxAp / CAP10

Table 1. AC ‘97 48-pin package pinlist

2.2 64-pin QFP package

The pinout for the 64-pin package is shown in Figure 5, package mechanicals are shown in Figure 6, and the pinlist is given in Table 2.

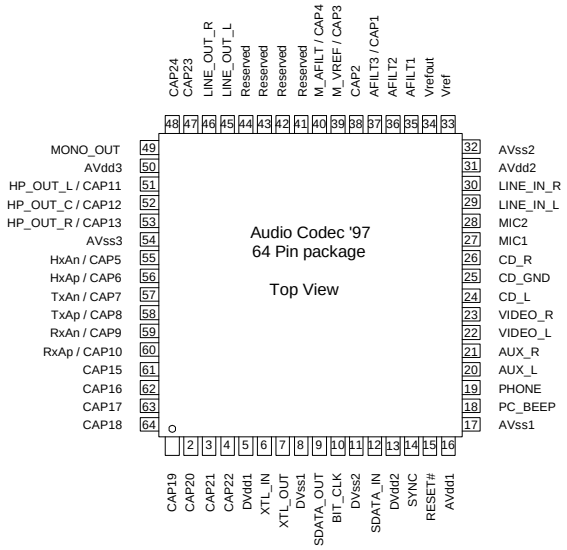
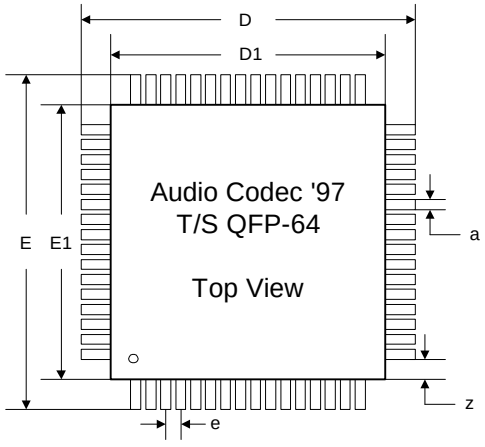


Figure 5. AC ‘97 64-pin package and pinout



Key	Dimension TQFP
D	12.00 mm
D1	10.00 mm
E	12.00 mm
E1	10.00 mm
a (lead width)	0.20 mm
e (pitch)	0.50 mm
z	1.00 mm

Figure 6. AC ‘97 64-pin package dimensions

Pin #	Signal Name	Pin#	Signal Name
1	CAP19	33	Vref
2	CAP20	34	Vrefout
3	CAP21	35	AFILT1
4	CAP22	36	AFILT2
5	DVdd1	37	AFILT3 / CAP1
6	XTL_IN	38	CAP2
7	XTL_OUT	39	M_VREF / CAP3
8	DVss1	40	M_AFILT/ CAP4
9	SDATA_OUT	41	LINE_OUT_LFE / CAP25
10	BIT_CLK	42	LINE_OUT_SURR_R / CAP26
11	DVss2	43	LINE_OUT_SURR_L / CAP27
12	SDATA_IN	44	LINE_OUT_CENTER / CAP28
13	DVdd2	45	LINE_OUT_L
14	SYNC	46	LINE_OUT_R
15	RESET#	47	CAP23
16	AVdd1	48	CAP24
17	AVss1	49	MONO_OUT
18	PC_BEEP	50	AVdd3
19	PHONE	51	HP_OUT_L / CAP11
20	AUX_L	52	HP_OUT_C / CAP12
21	AUX_R	53	HP_OUT_R / CAP13
22	VIDEO_L	54	AVss3
23	VIDEO_R	55	HxAn / CAP5
24	CD_L	56	HxAp / CAP6
25	CD_GND	57	TxAn / CAP7
26	CD_R	58	TxAp / CAP8
27	MIC1	59	RxAn / CAP9
28	MIC2	60	RxAp / CAP10
29	LINE_IN_L	61	CAP15
30	LINE_IN_R	62	CAP16
31	AVdd2	63	CAP17
32	AVss2	64	CAP18

Table 2. AC ‘97 64-pin package pinlist

3. Pin/Signal Descriptions

3.1. Digital I/O

These signals connect the AC ‘97 component to its controller counterpart and external crystal.

Signal Name	Type	Description
RESET#	I	AC ‘97 Master H/W Reset
XTL_IN	I	24.576 MHz Crystal
XTL_OUT	O	24.576 MHz Crystal
SYNC	I	48 KHz fixed rate sample sync
BIT_ CLK	O	12.288 MHz serial data clock
SDATA_OUT	I	Serial, time division multiplexed, AC ‘97 input stream
SDATA_IN	O	Serial, time division multiplexed, AC ‘97 output stream

Table 3. Digital Signal List

3.2. Analog I/O

These signals connect the AC ‘97 component to analog sources and sinks, including microphones and speakers.

Signal Name	Type	Description
PC_BEEP	I	PC Speaker beep pass through
PHONE	I	From telephony subsystem speakerphone (or DLP - Down Line Phone)
MIC1	I	Desktop Microphone Input
MIC2	I	Second Microphone Input
LINE_IN_L	I	Line In Left Channel
LINE_IN_R	I	Line In Right Channel
CD _L	I	CD Audio Left Channel
CD _GND	I	CD Audio analog ground
CD_ R	I	CD Audio Right Channel
VIDEO_L	I	Video Audio Left Channel
VIDEO_R	I	Video Audio Right Channel
AUX_L	I	Aux Left Channel
AUX_R	I	Aux Right Channel
LINE_OUT_L	O	Line Out Left Channel
LINE_OUT_R	O	Line Out Right Channel
HP_OUT_L / CAP11	O	Headphone Out Left Channel - optional
HP_OUT_C / CAP12	O	Headphone Out Common - optional
HP_OUT_R / CAP13	O	Headphone Out Right Channel - optional
MONO_OUT	O	To telephony subsystem speakerphone (or DLP - Down Line Phone)
HxAn / CAP5	O	Either Modem DAA - Hybrid interface or Generic Cap
HxAp / CAP6	O	Either Modem DAA - Hybrid interface or Generic Cap
TxAn / CAP7	O	Either Modem DAA - Hybrid interface or Generic Cap
TxAp / CAP8	O	Either Modem DAA - Hybrid interface or Generic Cap
RxAn / CAP9	I	Either Modem DAA - Hybrid interface or Generic Cap
RxAp / CAP10	I	Either Modem DAA - Hybrid interface or Generic Cap

Table 4. Analog Signal List

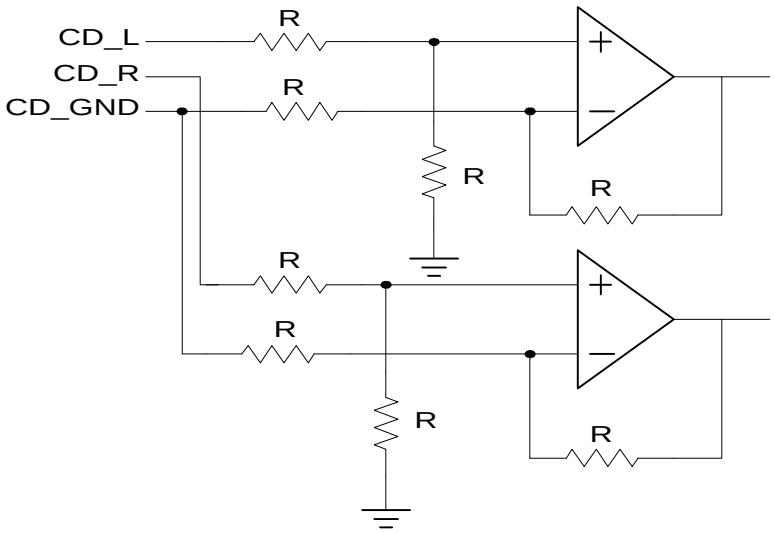


Figure 7. “Conceptual” example of CD circuit inside of AC ’97

3.3. Filter/References

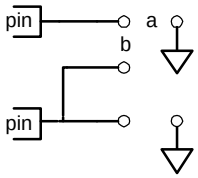
These signals are connected to resistors, capacitors, or specific voltages.

Signal Name	Type	Description
Vref	O	Reference Voltage
Vrefout	O	Reference Voltage out 5mA drive (intended for mic bias)
AFILT1	O	Anti-Aliasing Filter Cap - ADC channel
AFLIT2	O	Anti-Aliasing Filter Cap - ADC channel
AFILT3 / CAP1	O	Anti-Aliasing Filter Cap - optional Mic ADC channel
M_Vref / CAP3	O	Either Modem Reference Voltage or Generic Cap
M_AFILT / CAP4	O	Either Modem Anti-Aliasing Filter Cap or Generic Cap
HxAn / CAP5	O	Either Modem DAA - Hybrid interface or Generic Cap
HxAp / CAP6	O	Either Modem DAA - Hybrid interface or Generic Cap
TxAn / CAP7	O	Either Modem DAA - Hybrid interface or Generic Cap
TxAp / CAP8	O	Either Modem DAA - Hybrid interface or Generic Cap
RxAn / CAP9	O	Either Modem DAA - Hybrid interface or Generic Cap
RxAp / CAP10	O	Either Modem DAA - Hybrid interface or Generic Cap
HP_OUT_L / CAP11	O	Headphone out or Generic Cap
HP_OUT_C / CAP12	O	Headphone out or Generic Cap
HP_OUT_R / CAP13	O	Headphone out or Generic Cap
CAP2, CAP15-28	O	Generic Cap

Table 5. Filtering and Voltage References

The generic capacitor pins can be used internally to support 3D stereo enhancement, tone control, or other vendor specific functions. The specific use of each capacitor pin is left up to the AC ‘97 vendor. However, in order to support a vendor independent AC ‘97 layout, the following are recommended:

- internal functions which use generic capacitors between pins should always use odd-even (n, n+1) cap pairs, (i.e. 1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 15-16, 17-18, 19-20, 21-22, 23-24, 25-26, 27-28)
- internal functions which use generic capacitor to ground may use any cap, 1-28
- generic capacitor values should be no greater than 1uF (0805 package or smaller is preferred)



To configure capacitor to gnd:
a = capacitor, b = open
To configure capacitor pin to pin:
a = open, b = capacitor

Figure 8. Example of vendor independent external capacitor layout

3.4. Power and Ground Signals

It is recommended that the digital AC-link interface portion of the AC `97 component be capable of operating at either 5V or 3.3V, depending on which DVdd is supplied. For this reason the digital low and high level voltages are specified as percentages of DVdd (see DC Characteristics in Section 9). The following are clarifications:

- AC ‘97 digital runs at DVdd = 5V, DVdd = 3.3V, or either 5V or 3V (recommended).
- All DVdd inputs are the same level, 5V or 3.3V.
- When designed in the system AC '97 controller / AC '97 pairs always run off the same DVdd level.
- AC '97 analog runs at AVdd = 5V or AVdd = 3.3V.
- All AVdd inputs are the same level, 5V or 3.3V.
- DVdd and AVdd can be different levels.

Signal Name	Type	Description
AVdd1	I	Analog Vdd - 5.0V or 3.3V
AVdd2	I	Analog Vdd - 5.0V or 3.3V
AVdd3	I	Analog Vdd - 5.0V or 3.3V
AVss1	I	Analog Gnd
AVss2	I	Analog Gnd
AVss3	I	Analog Gnd
DVdd1	I	Digital Vdd - 5.0V, 3.3V, or either 5V or 3.3V
DVdd2	I	Digital Vdd - 5.0V, 3.3V, or either 5V or 3.3V
Dvss1	I	Digital Gnd
Dvss2	I	Digital Gnd

Table 6. Power Signal List

4. System Usage

4.1. AC ‘97 Connection to the Digital AC ’97 controller

AC ‘97 communicates with its companion AC ‘97 controller via a digital serial link, “AC-link”. All digital audio streams, optional modem line Codec streams, and command/status information are communicated over this point to point serial interconnect. A breakout of the signals connecting the two is shown in Figure 9. For a detailed description of the AC-link, the reader is referred to Section 5 of this specification.

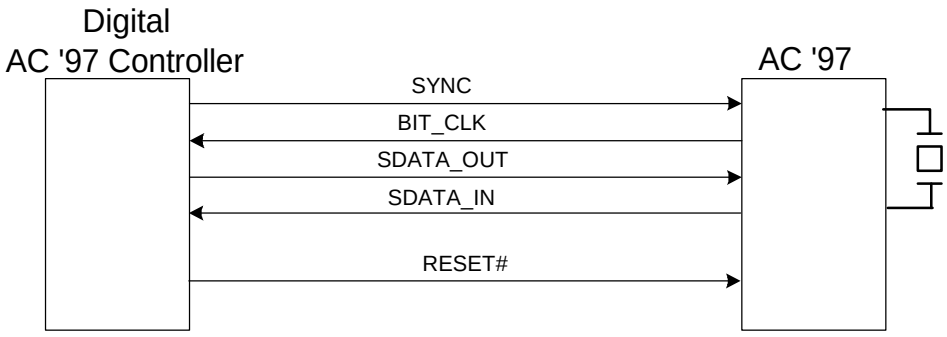


Figure 9. AC ‘97 connection to its companion AC ‘97 controller

4.2. Clocking

AC ‘97 derives its clock internally from an externally attached 24.576 MHz crystal[5], and drives a buffered and divided down (1/2) clock to its digital companion controller over AC-link under the signal name “BIT_CLK”. Clock jitter at the DACs and ADCs is a fundamental impediment to high quality output, and the internally generated clock will provide AC ‘97 with a clean clock that is independent of the physical proximity of AC ‘97’s companion digital controller (henceforth referred to as the “AC ’97 controller”).

The beginning of all audio sample packets, or “Audio Frames”, transferred over AC-link is synchronized to the rising edge of the “SYNC” signal. SYNC is driven by the AC ’97 controller. The AC ’97 controller takes BIT_CLK as an input and generates SYNC by dividing BIT_CLK by 256 and applying some conditioning to tailor its duty cycle. This yields a 48KHz SYNC signal whose period defines an audio frame. Data is transitioned on AC-link on every rising edge of BIT_CLK, and subsequently sampled on the receiving side of AC-link on each immediately following falling edge of BIT_CLK.

4.3. Resetting AC ‘97

There are 3 types of AC ‘97 reset:

1. a “cold” reset where all AC ‘97 logic (registers included) is initialized to its default state
2. a “warm” reset where the contents of the AC ‘97 register set are left unaltered
3. a “register” reset which only initializes the AC ‘97 registers to their default states

After signaling a reset to AC ‘97, the AC ’97 controller should not attempt to play or capture audio data until it has sampled a “Codec Ready” indication from AC ‘97. (Refer to section 5 for details)

[5] The use of crystal is recommended, but an external oscillator may also be input to AC ‘97 XTAL_IN

5. Digital Interface

5.1. AC-link Digital Serial Interface Protocol

AC ‘97 incorporates a 5 pin digital serial interface that links it to the AC ’97 controller. AC-link is a bi-directional, fixed rate, serial PCM digital stream. It handles multiple input, and output audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. With a minimum required DAC and ADC resolution of 16-bits, AC ‘97 could also be implemented with 18 or 20-bit DAC/ADC resolution, given the headroom that the AC-link architecture provides. The data streams currently defined by the AC ‘97 specification include:

- **PCM Playback** **2 output slots**
  2 channel composite PCM output stream
- **PCM Record data** **2 input slots**
  2 channel composite PCM input stream
- **Control** **2 output slots**
  Control register write port
- **Status** **2 input slots**
  Control register read port
- **Optional Modem Line Codec Output** **1 output slot**
  Modem line Codec DAC input stream
- **Optional Modem Line Codec Input** **1 input slot**
  Modem line Codec ADC output stream
- **Optional Dedicated Microphone Input** **1 input slot**
  Dedicated microphone input stream in support of stereo AEC, and/or other voice applications

Synchronization of all AC-link data transactions is signaled by the AC ’97 controller. AC ‘97 drives the serial bit clock onto AC-link, which the AC ’97 controller then qualifies with a synchronization signal to construct audio frames.

SYNC, fixed at 48 KHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data, AC ‘97 for outgoing data and AC ’97 controller for incoming data, samples each serial bit on the falling edges of BIT_CLK.

The AC-link protocol provides for a special 16-bit[6] time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A “1” in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is “tagged” invalid, it is the responsibility of the source of the data, (AC ‘97 for the input stream, AC ’97 controller for the output stream), to stuff all bit positions with 0’s during that slot’s active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the “Tag Phase”. The remainder of the audio frame where SYNC is low is defined as the “Data Phase”.

[6] 13-bits defined, with 3 reserved trailing bit positions.

Additionally, for power savings, all clock, sync, and data signals can be halted. This requires that AC ‘97 be implemented as a static design to allow its register contents to remain intact when entering a power savings mode.

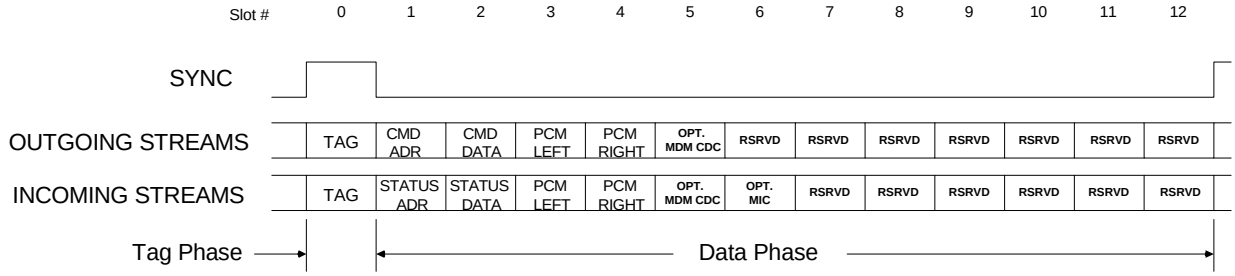


Figure 10. AC ‘97 Standard Bi-directional Audio Frame

5.1.1. AC-link Audio Output Frame (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting AC ‘97’s DAC inputs, and control registers. As briefly mentioned earlier, each audio output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16 bits which are used for AC-link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the “Valid Frame” bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12 bit positions sampled by AC ‘97 indicate which of the corresponding 12 time slots contain valid data. In this way data streams of differing sample rates can be transmitted across AC-link at its fixed 48 KHz audio frame rate[7]. The following diagram illustrates the time slot based AC-link protocol.

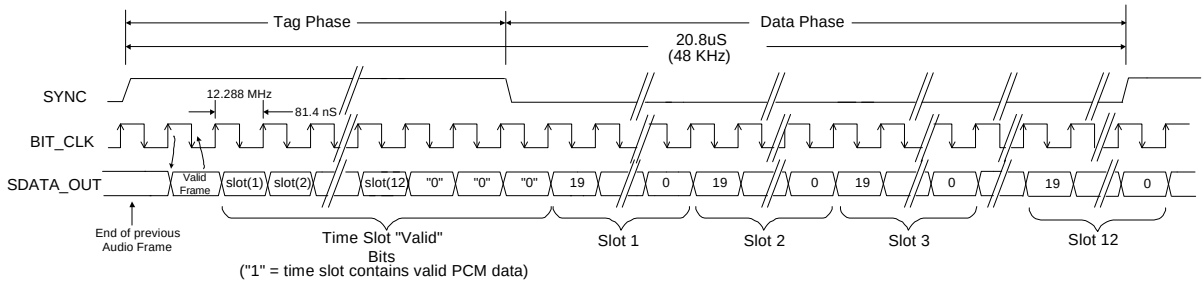


Figure 11. AC-link Audio Output Frame

A new audio output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, AC ‘97 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC ’97 controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled

[7] Control/Status as well as optional extensions of the baseline AC ‘97 specification, such as the modem line Codec, may take advantage of this feature. However baseline AC ‘97 specified audio functionality MUST ALWAYS sample rate convert to and from a fixed 48 Kss on the AC ’97 controller. This requirement is necessary to ensure that interoperability between AC ‘97 controller/AC ’97 pairs, among other things, can be guaranteed by definition for baseline specified AC ‘97 features.

by AC ‘97 on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

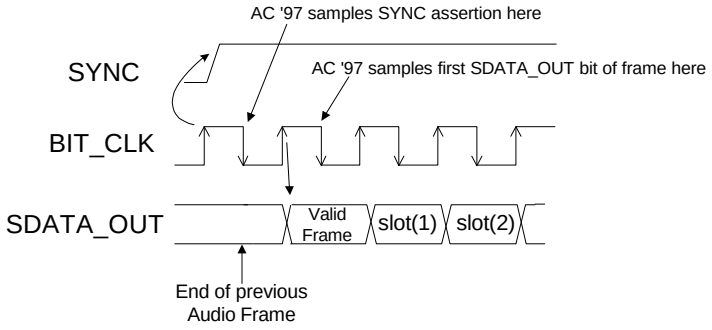


Figure 12. Start of an Audio Output Frame

SDATA_OUT’s composite stream is MSB justified (MSB first) with all non-valid slots’ bit positions stuffed with 0’s by the AC ’97 controller.

In the event that there are less than 20 valid bits within an assigned and valid time slot, the AC ’97 controller always stuffs all trailing non-valid bit positions of the 20-bit slot with 0’s.

As an example, consider an 8-bit sample stream that is being played out to one of AC ‘97’s DACs. The first 8-bit positions are presented to the DAC (MSB justified) followed by the next 12 bit-positions which are stuffed with 0’s by the AC ’97 controller. This ensures that regardless of the resolution of the implemented DAC (16, 18 or 20-bit), no DC biasing will be introduced by the least significant bits.

When mono audio sample streams are output from the AC ’97 controller it is necessary that BOTH left and right sample stream time slots be filled with the same data.

5.1.1.1. Slot 1: Command Address Port

The command port is used to control features, and monitor status (see Audio Input Frame Slots 1 and 2) for AC ‘97 functions including, but not limited to, mixer settings, and power management (refer to the control register section of this specification).

The control interface architecture supports up to 64 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid, odd register (01h, 03h, etc.) accesses are discouraged (if supported they should default to the preceeding even byte boundary - i.e. a read to 01h will return the 16-bit contents of 00h). Note that shadowing of the control register file on the AC ’97 controller is an option left open to the implementation of the AC ’97 controller. AC ‘97’s control register file is nonetheless required to be readable as well as writeable to provide more robust testability.

Audio output frame slot 1 communicates control register address, and write/read command information to AC ‘97.

Command Address Port bit assignments:

Bit(19)	Read/Write command	(1=read, 0=write)
Bit(18:12)	Control Register Index	(64 16-bit locations, addressed on even byte boundaries)
Bit(11:0)	Reserved	(Stuffed with 0’s)

The first bit (MSB) sampled by AC ‘97 indicates whether the current control transaction is a read or a write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be stuffed with 0’s by the AC ’97 controller.

5.1.1.2. Slot 2: Command Data Port

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle. (as indicated by Slot 1, bit 19)

Bit(19:4)	Control Register Write Data	(Stuffed with 0’s if current operation is a read)
Bit(3:0)	Reserved	(Stuffed with 0’s)

If the current command port operation is a read then the entire slot time must be stuffed with 0’s by the AC ’97 controller.

5.1.1.3. Slot 3: PCM Playback Left Channel

Audio output frame slot 3 is the composite digital audio left playback stream. In a typical ‘Games Compatible” PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC ’97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC ’97 controller must stuff all trailing non-valid bit positions within this time slot with 0’s.

5.1.1.4. Slot 4: PCM Playback Right Channel

Audio output frame slot 4 is the composite digital audio right playback stream. In a typical ‘Games Compatible” PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC ’97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC ’97 controller must stuff all trailing non-valid bit positions within this time slot with 0’s.

5.1.1.5. Slot 5: Optional Modem Line Codec

Audio output frame slot 5 contains the MSB justified modem DAC input data (if the line Codec is supported).

The optional modem DAC input resolution can be implemented as 16, 18 or 20-bits. At boot time, if the modem line codec is supported, the AC ’97 controller driver determines the DAC resolution. During normal runtime operation the AC ’97 controller is then responsible for stuffing any non-valid trailing bit positions within this time slot with 0’s.

Modem interoperability is not expected between AC `97 controller / AC `97 pairs that aren't sourced as a matched set by the same vendor. Given this, each vendor’s AC `97 controller implicitly knows what the Modem DAC/ADC resolution are in the AC `97 version w/ Modem support by inspecting the vendor ID registers.

5.1.1.6. Slots 6-12: Reserved

Audio output frame slots 6-12 are reserved for future use and are always stuffed with 0’s by the AC ’97 controller.

5.1.2. AC-link Audio Input Frame (SDATA_IN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC ’97 controller. As is the case for audio output frame, each AC-link audio input frame consists of 12, 20-bit time slots. Slot 0 is a special reserved time slot containing 16 bits which are used for AC-link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether AC ‘97 is in the “Codec Ready” state or not. If the “Codec Ready” bit is a 0, this indicates that AC ‘97 is not ready for normal operation. This condition is normal following the deassertion of power on reset for example, while AC ‘97’s voltage references settle. When the AC-link “Codec Ready” indicator bit is a 1 it indicates that the AC-link and AC ‘97 control and status registers are in a fully operational state. The AC ‘97 controller must further probe the Powerdown Control/Status Register (section 6.3) to determine exactly which subsections, if any, are ready.

Prior to any attempts at putting AC ‘97 into operation the AC ’97 controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that AC ‘97 has gone “Codec Ready”. Once AC ‘97 is sampled “Codec Ready”[8] then the next 12 bit positions sampled by the AC ’97 controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. The following diagram illustrates the time slot based AC-link protocol.

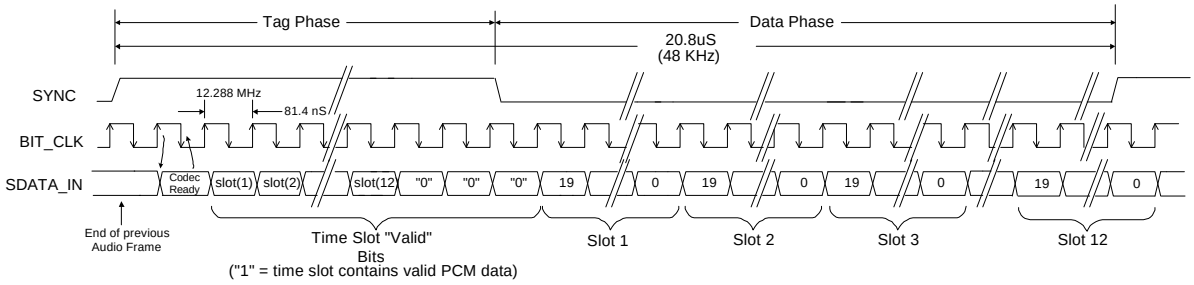


Figure 13. AC-link Audio Input Frame

A new audio input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, AC ‘97 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, AC ‘97 transitions SDATA_IN into the first bit position of slot 0 (“Codec Ready” bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AC ’97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

[8] There are several subsections within AC ‘97 that can independently go busy/ready. It is the responsibility of the AC ’97 controller to probe more deeply into the AC ‘97 register file to determine which AC ‘97 subsections are actually ready (refer to section 6.3).

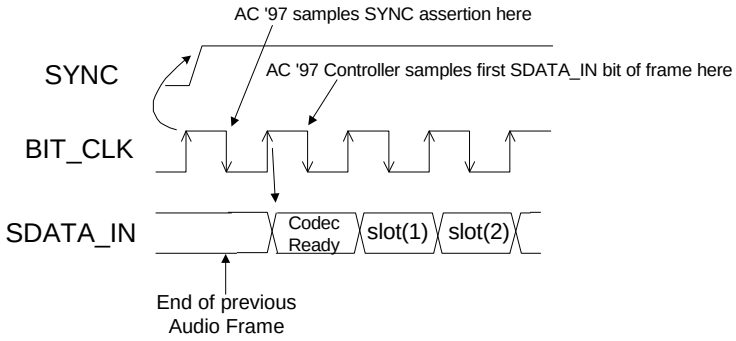


Figure 14. Start of an Audio Input Frame

SDATA_IN’s composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0’s by AC ‘97. SDATA_IN data is sampled on the falling edges of BIT_CLK .

5.1.2.1. Slot 1: Status Address Port

The status port is used to monitor status for AC ‘97 functions including, but not limited to, mixer settings, and power management (refer to section 6.3 of this specification).

Audio input frame slot 1’s stream echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged “valid” by AC ‘97 during slot 0)

Status Address Port bit assignments:

Bit(19)	RESERVED	(Stuffed with 0)
Bit(18:12)	Control Register Index	(Echo of register index for which data is being returned)
Bit(11:0)	RESERVED	(Stuffed with 0’s)

The first bit (MSB) generated by AC ‘97 is always stuffed with a 0. The following 7 bit positions communicate the associated control register address, and the trailing 12 bit positions are stuffed with 0’s by AC ‘97.

5.1.2.2. Slot 2: Status Data Port

The status data port delivers 16-bit control register read data.

Bit(19:4)	Control Register Read Data	(Stuffed with 0’s if tagged “invalid” by AC ‘97)
Bit(3:0)	RESERVED	(Stuffed with 0’s)

If Slot 2 is tagged “invalid” by AC ‘97, then the entire slot will be stuffed with 0’s by AC ‘97.

5.1.2.3. Slot 3: PCM Record Left Channel

Audio input frame slot 3 is the left channel output of AC ‘97’s input MUX, post-ADC.

AC ‘97’s ADCs can be implemented to support 16, 18, or 20-bit resolution.

AC ‘97 ships out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0’s to fill out its 20-bit time slot.

5.1.2.4. Slot 4: PCM Record Right Channel

Audio input frame slot 4 is the right channel output of AC ‘97’s input MUX, post-ADC.

AC ‘97’s ADCs can be implemented to support 16, 18, or 20-bit resolution.

AC ‘97 ships out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0’s to fill out its 20-bit time slot..

5.1.2.5. Slot 5: Optional Modem Line Codec

Audio input frame slot 5 contains MSB justified, modem ADC output data (if the line Codec is supported).

The optional modem ADC output resolution can be 16, 18, or 20-bits. All trailing non-valid bit positions will be stuffed with 0’s to fill out its 20-bit time slot.

Modem interoperability is not expected between AC `97 controller / AC `97 pairs that aren't sourced as a matched set by the same vendor. Given this, each vendor’s AC `97 controller implicitly knows what the Modem DAC/ADC resolution are in the AC `97 version w/ Modem support by inspecting the vendor ID registers.

5.1.2.6. Slot 6: Optional Dedicated Microphone Record Data

Audio input frame slot 6 is an optional (post-ADC) third PCM system input channel available for dedicated use by a desktop microphone. This input channel would supplement a true stereo output which would then enable a more precise echo cancellation algorithm for speakerphone applications.

AC ‘97’s ADCs can be implemented to support 16, 18, or 20-bit output resolution. Resolution of all PCM input ADC’s, including this optional Mic ADC is reported by the Reset register. If supported AC ‘97 will ship out ADC data of the implemented resolution (MSB first), and stuff any trailing non-valid bit positions with 0’s.

AC ‘97 controller/AC ’97 pair interoperability can only be guaranteed for non-optional AC ‘97 audio features. An audio component vendor who develops an AC ’97 with optional Dedicated Mic channel support should also offer an AC ’97 controller to fully support this feature with a matched set solution..

5.1.2.7. Slots 7-12: Reserved

Audio input frame slots 7-12 are reserved for future use and are always stuffed with 0’s by AC ‘97.

5.2. AC-link Low Power Mode

The AC-link signals can be placed in a low power mode (see section 6.3.). When AC ‘97’s Powerdown Register (26h), is programmed to the appropriate value, both BIT_CLK and SDATA_IN will be brought to, and held at a logic low voltage level.

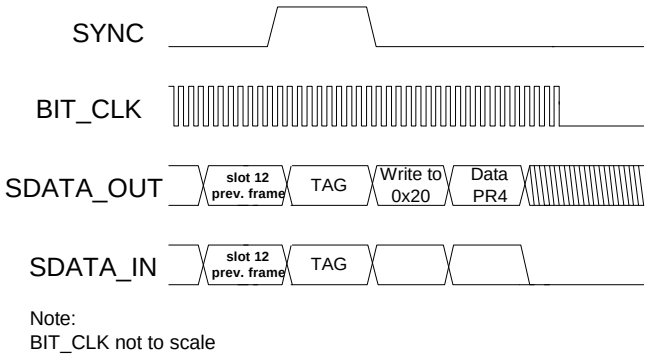


Figure 15. AC-link Powerdown Timing

BIT_CLK and SDATA_IN are transitioned low immediately[9] following the decode of the write to the Powerdown Register (26h) with PR4. When the AC ’97 controller driver is at the point where it is ready to program the AC-link into its low power mode, slots (1 and 2) ARE ASSUMED TO BE the only valid stream in the audio output frame[10].

The AC ’97 controller should also drive SYNC, and SDATA_OUT low after programming AC ‘97 to this low power, “halted” mode.

Once AC ‘97 has been instructed to halt BIT_CLK, a special “wake up” protocol must be used to bring the AC-link to the active mode since normal audio output and input frames can not be communicated in the absence of BIT_CLK.

5.2.1. Waking up the AC-link

There are 2 methods for bringing the AC-link out of a low power, halted mode. Regardless of the method, it is the AC ’97 controller that performs the wake up task.

AC-link protocol provides for a “Cold AC ‘97 Reset”, and a “Warm AC ‘97 Reset”. The current power down state would ultimately dictate which form of AC ‘97 reset is appropriate. Unless a “cold” or “register” reset (a write to the Reset register) is performed, wherein the AC ‘97 registers are initialized to their default values, registers are required to keep state during all power down modes.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of 4 audio frame times following the frame in which the power down was triggered. When AC-link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

[9] Within the maximun specified time.
[10] At this point in time it is assumed that all sources of audio input have also been neutralized.

5.2.1.1. Cold AC ‘97 Reset

A cold reset is achieved by asserting RESET# for the minimum specified time. By driving RESET# low, BIT_CLK, and SDATA_OUT will be activated, or re-activated as the case may be, and all AC ‘97 control registers will be initialized to their default power on reset values.

RESET# is an asynchronous AC ‘97 input.

5.2.1.2. Warm AC ‘97 Reset

A warm AC ‘97 reset will re-activate the AC-link without altering the current AC ‘97 register values. A warm reset is signaled by driving SYNC high for a minimum of 1uS in the absence of BIT_CLK.

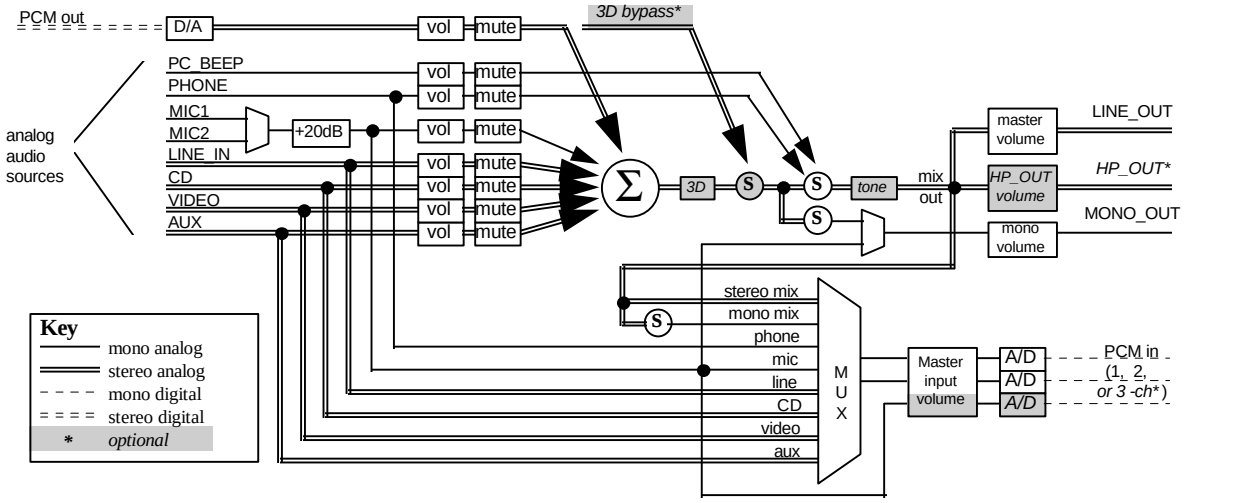
Within normal audio frames SYNC is a synchronous AC ‘97 input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to AC ‘97.

AC ‘97 MUST NOT respond with the activation of BIT_CLK until SYNC has been sampled low again by AC ‘97. This will preclude the false detection of a new audio frame.

6. AC '97 Mixer

The AC '97 mixer is designed to manage playback and record of all digital and analog audio sources likely to be present in the 1997 high volume PC. These include:

- **System audio**: digital PCM input and output for business, games, and multimedia
- **CD/DVD:** analog CD/DVD-ROM Redbook audio with internal connections to Codec mixer
- **Mono microphone**: choice of desktop or headset mic, with programmable boost and gain
- **Speakerphone**: use of system mic & speakers for telephony, DSVD, and video conferencing
- **Stereo line in**: analog external line level source from consumer audio, video camera, etc
- **Video:** TV tuner or video capture card with internal connections to Codec mixer
- **AUX/synth**: analog FM or wavetable synthesizer, or other internal source



source	function	connection
PC_BEEP	PC beep pass thru	from PC beeper output
PHONE	speakerphone or DLP in	from telephony subsystem
MIC1	desktop microphone	from mic jack
MIC2	headset microphone	from headset mic jack
LINE_IN	external audio source	from line in jack
CD	audio from CD-ROM drive	cable from CD-ROM
VIDEO	audio from TV tuner or video camera	cable from TV or VidCap card
AUX	upgrade synth or other external source	internal connector
PCM out	digital audio output from AC '97 Controller	AC-link
mix out	mix of all sources	AC '97 internal
LINE_OUT	stereo mix of all sources	to output jack
HP_OUT	stereo mix of all sources	to headphone jack
MONO_OUT	mic or mix for speakerphone or DLP out	to telephony subsystem
PCM in	digital audio input to AC '97 Controller	AC-link

Output MIX supports:
- stereo mix of all sources for LINE_OUT
- mono mic or mix for MONO_OUT
- *optional HP_OUT for headphone**
- *optional 3D and tone control**
- *PCM out can be mixed pre or post 3D**

Input MUX supports:
- select from 1, 2, *or 3** channels
- any mono or stereo source
- mono or stereo mix of all sources
- 2-ch input w/ output ref (mic + mono mix)
- *3rd channel dedicated to mic**
- *3-ch input w/ output ref (mic + stereo mix)**

Figure 16. AC '97 Mixer Functional Diagram

6.1. Mixer output

The AC ‘97 mixer generates two distinct outputs:

- a stereo mix of all sources for output to the speakers, headset, and line out (LINE_OUT and HP_OUT)
- a mono, mic only or mix of all sources (minus PHONE and PC_BEEP) for speakerphone out (MONO_OUT)

6.1.1. PCM out path and optional 3D bypass

If analog 3D stereo enhancement is supported in AC ‘97 it is desirable that the PCM out source be mixable pre or post analog 3D processing. This allows digital 3D audio (rendered with volume, pan, reverb, Doppler, HRTF, etc.) on PCM out to bypass the analog 3D processing regardless of whether analog 3D is enabled or disabled. This prevents “smearing” of digital 3D audio, and also enables digital 3D audio sources to be mixed with 3D stereo enhanced analog sources (CD, AUX, etc).

The default PCM out path is through volume, mute, and analog 3D stereo enhancement. However, if the AC ’97 controller implements digital 3D audio, and detects analog 3D stereo enhancement support in the AC ’97 analog, it can enable the 3D bypass path. This capability to switch to post 3D can also be exposed via API’s to support SW which emulates or accelerates digital 3D rendering.

In either PCM out scenario it is advantageous for the AC ‘97 controller to use the post D/A analog volume control to support full resolution D/A conversions followed by analog attenuation as a means of achieving high SNR.

6.2. Mixer input

The mixer input is a MUX design which offers the capability to record any of the audio sources or the outgoing mix of all sources. This design is more efficient to implement than an independent input mix, allows the user to apply 3D and tone controls to recordings, and offers simple monitoring when a mix is recorded: what you hear is what you get (WYHIWYG). Mono and stereo mix also provide excellent echo cancellation reference signals.

AC ‘97 supports the full range of input options[11]:

- any mono or stereo source
- mono or stereo mix of all sources
- 2-channel input w/ mono output reference (mic + mono mix for mono echo cancellation)
- optional 3-channel input w/ stereo output reference (mic + stereo mix for stereo echo cancellation)

[11] The audio driver should maintain a persistent record input level for each MUX input option.

6.3. Mixer Registers

The register indexes and usage are shown below in Table 1. All registers not shown and bits containing an X are assumed to be reserved.

Table 7. Mixer Registers

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	na
02h	Master Volume	Mute	X	*ML5*	ML4	ML3	ML2	ML1	ML0	X	X	*MR5*	MR4	MR3	MR2	MR1	MR0	8000h
04h*	Headphone Volume	Mute	X	*ML5*	ML4	ML3	ML2	ML1	ML0	X	X	*MR5*	MR4	MR3	MR2	MR1	MR0	8000h
06h	Master Volume Mono	Mute	X	X	X	X	X	X	X	X	X	*MM5*	MM4	MM3	MM2	MM1	MM0	8000h
08h*	Master tone (R & L)	X	X	X	X	BA3	BA2	BA1	*BA0*	X	X	X	X	TR3	TR2	TR1	*TR0*	0F0Fh
0Ah	PC_BEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV2	PV0	X	x000h
0Ch	Phone Volume	Mute	X	X	X	X	X	X	X	X	X	*GN5*	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20dB	*GN5*	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Vol	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
1Eh*	Record Gain Mic	Mute	X	X	X	X	X	X	X	X	X	X	X	GM3	GM2	GM1	GM0	8000h
20h	General Purpose	*POP*	ST	3D	LD	*LLBK*	*RLBK*	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
22h*	3D Control	X	X	X	X	CR3	CR2	CR1	CR0	X	X	X	X	DP3	DP2	DP1	DP0	0000h
24h*	Modem Rate	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000h
26h	Powerdown Ctrl/Stat	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	MDM	REF	ANL	DAC	ADC	na
28h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..
5Ah	Vendor Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..
7Ah	Vendor Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	na
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	na

NOTES:

1. * indicates optional feature registers. Whether implemented or not, these can always be written to, but reads will be don't care if there is no support for the feature.
2. *ITALIC UNDERLINE* indicates optional bits within a register.
3. Any reserved bits, marked X, can be written to but are don't care upon read back.
4. PC_BEEP default can be 0000h or 8000h, mute off or on.

6.3.1. Reset Register (Index 00h)

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the ID code of the part and a code for the type of 3D Stereo Enhancement, if any.

All DACs operate at the same resolution. All ADCs operate at the same resolution. The only possible exceptions are the Modem ADC and DAC. Modem interoperability is not expected between AC `97 controller / AC `97 pairs that aren't sourced as a matched set by the same vendor. Given this, each vendor’s AC `97 controller implicitly knows what the Modem DAC/ADC resolution are in the AC `97 version w/ Modem support by inspecting the vendor ID registers.

The ID decodes the capabilities of AC ‘97 based on the following:

Bit = 1	Function
ID0	Dedicated Mic PCM In channel
ID1	Modem Line Codec support
ID2	Bass & Treble control
ID3	Simulated Stereo (Mono to Stereo)
ID4	Headphone out support
ID5	Loudness (bass boost) support
ID6	18 bit DAC resolution
ID7	20 bit DAC resolution
ID8	18 bit ADC resolution
ID9	20 bit ADC resolution

The 3D stereo enhancement decodes are based on the following: Note that the 3D control register defines 2 16-step controls for the 3D Stereo Enhancement function. These controls can be used to support center and depth, but can also be used generically. The 3D control register should be read to determine if the selected enhancement is either fixed or variable center and depth. If the lower 8-bits of the 3D control register are non-zero, then the depth/generic1 control is fixed, otherwise it is variable. If the upper 8-bits of the 3D control register are non-zero, then center/generic2 control is fixed, otherwise it is variable.

SE4...SE0	3D Stereo Enhancement Technique	SE4...SE0	3D Stereo Enhancement Technique
00000 (0)	No 3D Stereo Enhancement	01011(11)	AKM* 3D Audio
00001 (1)	Analog Devices* Phat Stereo	01100 (12)	Aureal* Stereo Enhancement
00010 (2)	Creative Stereo Enhancement	01101 (13)	AZTECH* 3D ENHANCEMENT
00011 (3)	National Semiconductor* 3D Stereo Enhancement	01110 (14)	Binaura* 3D Audio Enhamcement
00100 (4)	YAMAHA* Ymersion	01111 (15)	ESS Technology* (stereo enhancement)
00101 (5)	BBE* 3D Stereo Enhancement	10000 (16)	Harman International* VMAx
00110 (6)	Crystal Semiconductor* 3D Stereo Enhancement	10001 (17)	NVidea* 3D Stereo Enhancement
00111 (7)	Qsound* QXpander	10010 (18)	Philips* Incredible Sound
01000 (8)	Spatializer* 3D Stereo Enhancement	10011 (19)	Texas Instruments* 3D Stereo Enhancement
01001 (9)	SRS* 3D Stereo Enhancement	10100 (20)	VLSI Technology* 3D Stereo Enhancement

01010 (10)	Platform Technologies* 3D Stereo Enhancement		

6.3.2. Play Master Volume Registers (Index 02h, 04h and 06h)

These registers manage the output signal volumes. **Register 02h** controls the stereo master volume (both right and left channels), **Register 04h** controls the optional stereo headphone out, **Register 06h** controls the mono volume output. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. ML5 through ML0 is for left channel level, MR5 through MR0 is for the right channel and MM5 through MM0 is for the mono out channel.

Support for the MSB of the level is optional. **If the MSB is not supported then AC ‘97 needs to detect when that bit is set and set all 4 LSBs to 1s.** Example: If AC ‘97 only supports 5 bits of resolution in its mixer and the driver writes a 1xxxxx AC ‘97 must interpret that as x11111. It will also respond when read with x11111 rather then 1xxxxx, the value writen to it. The driver can use this feature to detect if support for the 6th bit is there or not.

The default value is 8000h (1000 0000 0000 0000), which corresponds to 0 dB attenuation with mute on.

Mute	M*x*5...M*x*0	Function	Range
0	00 0000	0dB Attenuation	Req.
0	01 1111	46.5dB Attenuation	Req.
0	11 1111	94.5dB Attenuation	Optional
1	xx xxxx	∞ dB Attenuation	Req.

6.3.3. Master Tone Control Registers (Index 08h) - *Optional*

Optional register for support of tone controls (bass and treble). If the part does not support bass and treble writing to this register will have no effect and reading will result in all don’t care values. The step size is 3dB with optional support for 1.5dB. The step size option is accomplished by either using 3 bits (MSB justified) for 3dB steps or all 4 bits for 1.5dB steps. Writing a 0000h corresponds to +10.5dB of gain. Center frequencies (which gains are measured from) are 100Hz for Bass and 10,000Hz for Treble. The default value is 0F0Fh, which corresponds to bypass of bass or treble gain.

TR3...*TR0* or BA3...*BA0*	Req support	Function
000*0*	yes	+10.5dB of gain
000*1*	no	+9dB of gain
001*0*	yes	+7.5dB of gain
001*1*	no	+6dB of gain
..		...
011*0*	yes	+1.5dB of gain
011*1*	yes	0 dB of gain
100*0*	yes	-1.5dB of gain
..		...
110*0*	yes	-7.5dB

110*1*	no	-9dB of gain
111*0*	yes	-10.5dB of gain
111*1*	yes	Bypass

6.3.4. PC Beep Register (Index 0Ah)

This controls the level for the PC Beep input. Each step corresponds to approximately 3dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB.

PC_BEEP supports motherboard AC ‘97 Controller /Codec implementations. The intention of routing PC_BEEP through the Codec analog mixer is to eliminate the requirement for an onboard speaker or piezoelectric device by guaranteeing a connection to speakers connected via the output jack. In order for this to be viable the PC_BEEP signal needs to reach the output jack at all times, with or without the audio driver's support.

NOTE: The PC_BEEP is recommended to be routed to L & R Line outputs even when AC ‘97 is in a RESET State. This is so that Power On Self Test (POST) codes can be heard by the user in case of a hardware problem with the PC. This can be accomplished with a high impedance path to the outputs without any attenuation. For further PC_BEEP implementation details please refer to the AC ‘97 Technical FAQ sheet.

The default value can be 0000h or 8000h, which corresponds to 0 dB attenuation with mute off or on.

Mute	PV3...PV0	Function
0	0000	0dB Attenuation
0	1111	45dB Attenuation
1	xxxx	∞ dB Attenuation

6.3.5. Analog Mixer Input Gain Registers (Index 0Ch - 18h)

This controls the gain/attenuation for each of the analog inputs. Each step corresponds to approximately 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB.

- **Register 0Eh** (Mic Volume Register) has an extra bit that is for a 20dB boost. When bit 6 is set to 1 the 20dB boost is on. The default value is 8008, which corresponds to 0 dB gain with mute on.

The default value for the mono registers is 8008h, which corresponds to 0dB gain with mute on. The default value for stereo registers is 8808h, which corresponds to 0dB gain with mute on.

Mute	G*x*4...G*x*0	Function
0	00000	+12dB gain
0	01000	0dB gain
0	11111	-34.5dB gain
1	xxxxx	–∞ dB gain

6.3.6. Record Select Control Register (Index 1Ah)

Used to select the record source independently for right and left. See table for legend.

The default value is 0000h, which corresponds to Mic in.

SR2...SR0	Right Record Source
0	Mic
1	CD In (R)
2	Video In (R)
3	Aux In (R)
4	Line In (R)
5	Stereo Mix (R)
6	Mono Mix
7	Phone

SL2...SL0	Left Record Source
0	Mic
1	CD In (L)
2	Video In (L)
3	Aux In (L)
4	Line In (L)
5	Stereo Mix (L)
6	Mono Mix
7	Phone

6.3.7. Record Gain Registers (Index 1Ch and 1Eh)

1Ch is for the stereo input and 1Eh is for the optional special purpose correlated audio mic channel. Each step corresponds to 1.5 dB. 22.5dB corresponds to 0F0Fh and 000Fh respectively. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel(s) is set at -∞ dB.

The default value is 8000h, which corresponds to 0 dB gain with mute on.

Mute	G*x*3...G*x*0	Function
0	1111	+22.5 dB gain
0	0000	0dB gain
1	xxxxx	–∞ dB gain

6.3.8. General Purpose Register (Index 20h)

This register is used to control several miscellaneous functions of the AC '97 component. Below is a summary of each bit and its function. The *POP* bit controls the optional PCM out 3D bypass path (the pre and post 3D PCM out paths are mutually exclusive). The MS bit controls the mic selector. The Loudness (bass boost) bit is to control an optional loudness contour or "bass boost" function. The exact implementation of this is left up to the vendor. This register should be read before writing to generate a mask for only the bit(s) that need to be changed. The function default value is 0000h which is all off. The LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-link, allowing for full system performance measurements.

Bit	Function
POP	*PCM out path & mute, 0 = pre 3D, 1 = post 3D*
ST	*Simulated Stereo Enhancement on/off 1 = on*
3D	*3D Stereo Enhancement on/off 1 = on*
LD	*Loudness (bass boost) on/off 1 = on*
LLBK	*Local Loop Back - For Modem Line Codec*
RLBK	*Remote Loop Back - For Modem Line Codec*
MIX	Mono output select 0=Mix, 1=Mic
MS	Mic select 0 = Mic1, 1= Mic2
LPBK	ADC/DAC loopback mode

6.3.9. 3D Control Register (Index 22h) - *Optional*

This optional register is used to control the center and/or depth of the 3D stereo enhancement function built into of the AC '97 component. Note this register should be read to indicate if the selected 3D stereo enhancement is of either fixed or variable center and depth. If this control register is non-zero then the enhancement is fixed. The register default value is either the fixed value or 0000h if it is variable. Linear or logarithmic implementation is acceptable, depending on the 3D technology (linear is shown below):

CR3...CR0 DP3...DP0	Center Depth
0	0%
1	6.67%
.	.
.	.
14	93.33%
15	100%

6.3.10. Modem Sample Rate Register (Index 24h)

This register controls what sample rate AC '97 is sending or receiving samples for Modem in & out. The rate is a 16 bit unsigned integer that specifies the rate with resolution down to 1 Hz. R15 is MSB and R0 is the LSB of the 16 bit integer value. The modem rate is always the same for input and output. Any rate over 48KHz is not allowed as the max rate is 48K.

6.3.11. Powerdown Control/Status Register (Index 26h)

This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status, a "1" indicating that the subsection is "*ready*". *Ready* is defined as the subsection able to perform in its nominal state. When this register is written the bit values that come in on AC-link will have no effect on read only bits 0-7.

When the AC-link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1 it indicates that the AC-link and AC '97 control and status registers are in a fully operational state. The AC '97 controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any, are ready.

Bit	Function
MDM	Modem section ready
REF	Vref's up to nominal level
ANL	Analog mixers, etc ready
DAC	DAC section ready to accept data
ADC	ADC section ready to transmit data

The power down modes are as follows. The first three bits are to be used individually rather than in combination with each other. The last bit PR3 can be used in combination with PR2 or by itself. PR0 and PR1 control the PCM ADC's and DAC's only, PR7 independently controls the optional modem ADC and DAC.

Bit	Function
PR0	PCM in ADC's & Input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analog Mixer powerdown (Vref still on)
PR3	Analog Mixer powerdown (Vref off)
PR4	Digital Interface (AC-link) powerdown (external clk off)
PR5	Internal Clk disable
PR6	HP amp powerdown
PR7	Modem ADC/DAC off - if supported

6.3.12. Reserved Registers (Index 28h - 58h)

These are reserved. Do not write to these registers.

6.3.13. Vendor Reserved Registers (Index 5Ah - 7Ah)

These are reserved for future use and are vendor specific. Do not write to these registers unless the Vendor ID register has been checked first to ensure that the driver knows the source of the AC ‘97 component.

6.3.14. Vendor ID Registers (Index 7Ch - 7Eh)

This register is for specific vendor identification if so desired. The ID method is Microsoft’s Plug and Play Vendor ID code with F7..0 the first character of that id, S7..0 the second character and T7..0 the third character. These three characters are ASCII encoded. The REV7..0 field is for the Vendor Revision number.

7. Low Power Modes

AC ‘97 is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). There are 7 commands of separate power down with the addition of the Modem Codec. See the table below for the different modes. AC ‘97 is assumed to be a fully static design, that is if the clock is stopped the registers will not lose their values.

GPR Bits	Function
PR0	PCM in ADC’s & Input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analog Mixer powerdown (Vref still on)
PR3	Analog Mixer powerdown (Vref off)
PR4	Digital Interface (AC-link) powerdown (external clk off)
PR5	Internal Clk disable
PR6	HP amp powerdown
PR7	Modem ADC/DAC off - if supported

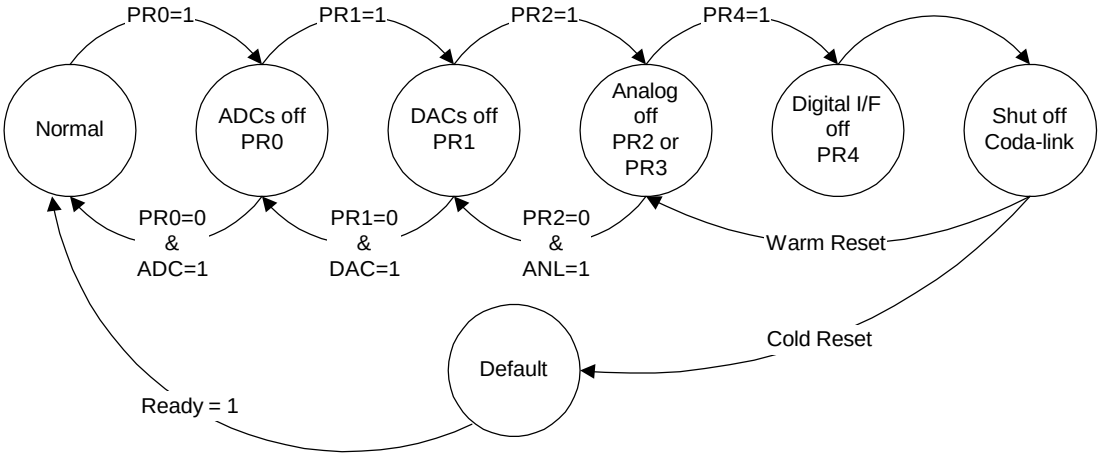


Figure 17. One example of AC ‘97 Powerdown/Powerup flow

The above figure illustrates one example procedure to do a complete powerdown of AC ‘97. From normal operation sequential writes to the Powerdown Register are performed to power down AC ‘97 a piece at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC ‘97’s digital interface (AC-link). The part will remain in sleep mode with all its registers holding their static values. To wake up, the AC ‘97 controller will send pulse on the sync line issuing a warm reset. This will restart AC ‘97’s digital interface (resetting PR4 to zero). AC ‘97 can also be woken up with a cold reset. A cold reset will cause a loss of values of the registers as a cold reset will set them to their default states. When a section is powered back on the

Powerdown Control/Status register (index 26h) should be read to verify that the section is ready (i.e. stable) before attempting any operation that requires it.

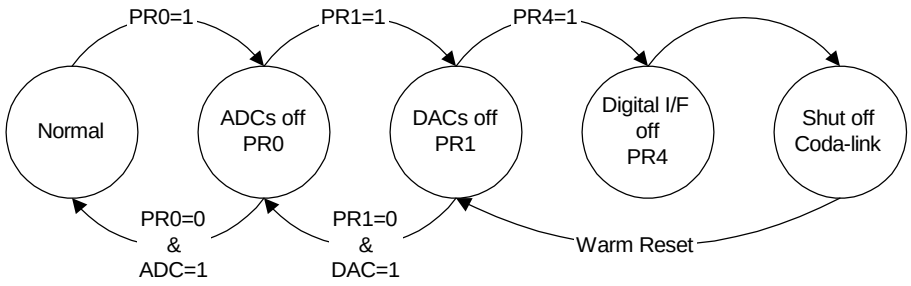


Figure 18. AC ‘97 Powerdown/Powerup flow with analog still alive

The above figure illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This is used when the user could be playing a CD (or external LINE_IN source) through AC ‘97 to the speakers but have most of the system in low power mode. The procedure for this follows the previous except that the analog mixer is never shut down.

8. Testability

8.1. Activating the Test Modes

AC ‘97 has two test modes. One is for ATE in circuit test and the other is for vendor specific tests. AC ‘97 enters the ATE in circuit test mode if SDATA_OUT is sampled high at the trailing edge of RESET#. AC ‘97 enters the vendor specific test mode when coming out of RESET if SYNC is high. These cases will never occur during standard operating conditions.

Regardless of the test mode, the AC ‘97 controller must issue a “cold” reset to resume normal operation of the AC ‘97 Codec.

8.2. Test Mode Functions

8.2.1 ATE in circuit test mode

When AC ‘97 is placed in the ATE test mode, its digital AC-link outputs (i.e. BIT_CLK and SDATA_IN) are driven to a high impedence state. This allows ATE in circuit testing of the AC ‘97 controller.

8.2.2 Vendor Specific test mode

To be left up to the individual vendors.

9. AC-link Digital DC and AC Characteristics

9.1. DC Characteristics

($T_{ambient}$ = 25^{0}C, AVdd = DVdd = 5.0V or 3.3V +/- 5%; AVss = DVss = 0V; 50pF external load)

Parameter	Symbol	Min	Typ	Max	Units
Input voltage range	V_{in}	-0.30	-	DVdd + 0.30	V
Low level input voltage	V_{il}	-	-	0.30 x Vdd	V
High level input voltage	V_{ih}	0.40 x Vdd	-	-	V
High level output voltage	V_{oh}	0.50 x Vdd	-	-	V
Low level output voltage	V_{ol}	-	-	0.20 x Vdd	V
Input Leakage Current (AC-link inputs)	-	-10	-	10	uA
Output Leakage Current (Hi-Z’d AC-link outputs)	-	-10	-	10	uA
Output buffer drive current	-	-	5	-	mA

NOTE: It is recommended that the digital portion of the AC ‘97 component be capable of operating at either 5.0V or 3.3V (+/- 5%), depending on which DVdd is supplied (see section 3.4 for description of Power and Ground Signal levels).

In order to specify operation of the digital portion of the AC '97 component at both 5.0 V and 3.3 V, the low and high level input and output voltages are specified as percentages of the digital supply voltage. The AC ‘97 Working Group believes that it is possible to deliver dual voltage parts which meet the above specification. However, the following has been added to simplify the implementation for those who do not support dual voltage (and possibly those who do), by allowing 5.0 or 3.3 V parts to match the PCI 2.1 specifications for V_{ih}, V_{il}, V_{oh}, and V_{ol}:

5.0 V Only Operation					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Input voltage range	V_{in}	-0.30	-	5.30	V
Low level input voltage	V_{il}	-	-	0.8	V
High level input voltage	V_{ih}	2.0	-	-	V
High level output voltage	V_{oh}	2.4	-	-	V
Low level output voltage	V_{ol}	-	-	.55	V

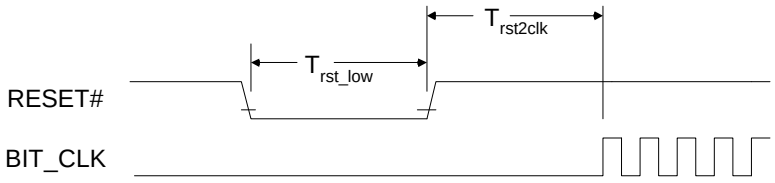
3.3 V Only Operation					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Input voltage range	V_{in}	-0.30	-	3.60	V
Low level input voltage	V_{il}	-	-	1.0	V
High level input voltage	V_{ih}	1.6	-	-	V
High level output voltage	V_{oh}	2.97	-	-	V
Low level output voltage	V_{ol}	-	-	0.33	V

9.2. AC Timing Characteristics

($T_{ambient}$ = 25^0C, AVdd = DVdd = 5VDC or 3.3VDC; AVss = DVss = 0V; 50pF external load)

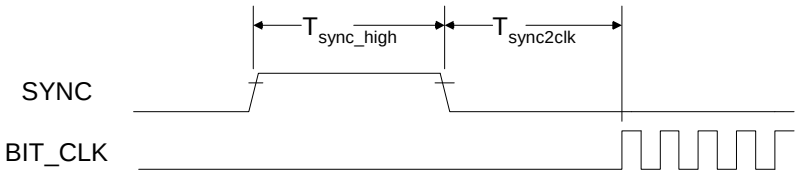
9.2.1. Reset

9.2.1.1. Cold Reset



Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	uS
RESET# inactive to BIT_CLK startup delay	$T_{rst2clk}$	162.8	-	-	nS

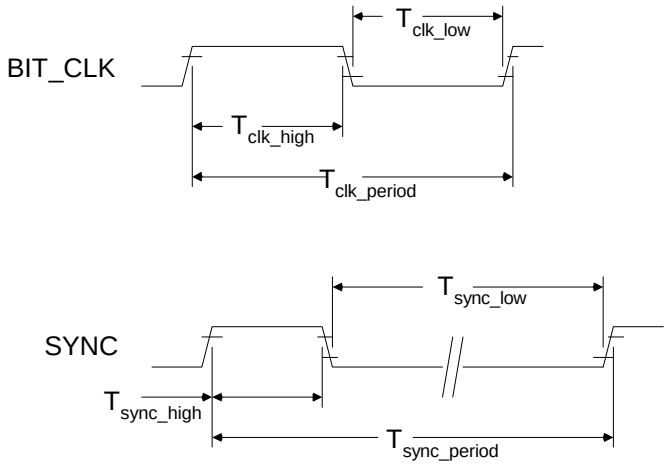
9.2.1.2. Warm Reset



Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	T_{sync_high}	-	1.3	-	uS
SYNC inactive to BIT_CLK startup delay	$T_{sync2clk}$	162.8	-	-	nS

9.2.2. Clocks

(50pF external load)

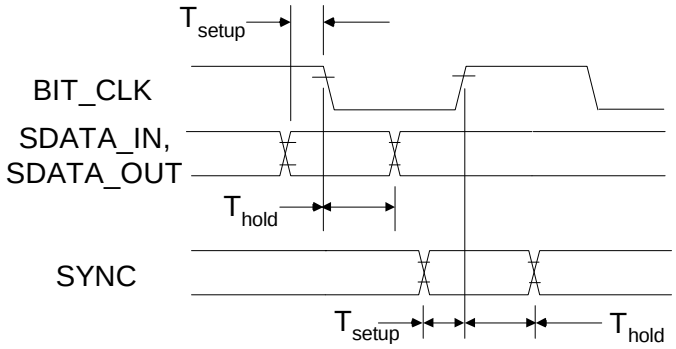


Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	nS
BIT_CLK output jitter		-	-	750	pS
BIT_CLK high pulse width (note 1)	T_{clk_high}	32.56	40.7	48.84	nS
BIT_CLK low pulse width (note 1)	T_{clk_low}	32.56	40.7	48.84	nS
SYNC frequency		-	48.0	-	KHz
SYNC period	T_{sync_period}	-	20.8	-	uS
SYNC high pulse width	T_{sync_high}	-	1.3	-	uS
SYNC low pulse width	T_{sync_low}	-	19.5	-	uS

Notes:
1) Worst case duty cycle restricted to 40/60.

9.2.3. Data Setup And Hold

(50pF external load)

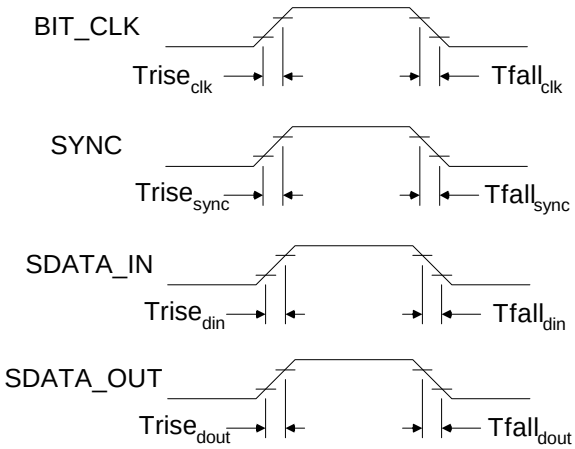


Parameter	Symbol	Min	Typ	Max	Units
Setup to falling edge of BIT_CLK	T_{setup}	15.0	-	-	nS
Hold from falling edge of BIT_CLK	T_{hold}	5.0	-	-	nS

Note 1: Setup and hold time parameters for SDATA_IN are with respect to the AC ‘97 Controller.

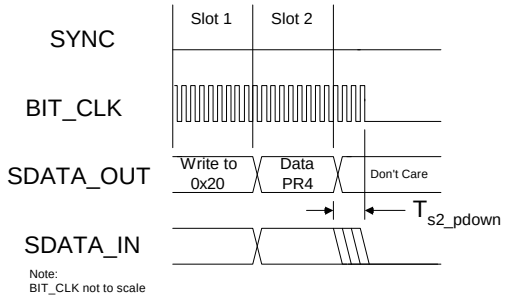
9.2.4. Signal Rise and Fall Times

(50pF external load; from 10% to 90% of Vdd)



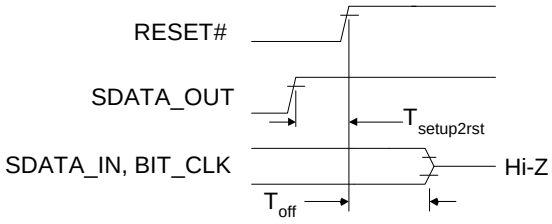
Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	$Trise_{clk}$	2	-	6	nS
BIT_CLK fall time	$Tfall_{clk}$	2	-	6	nS
SYNC rise time	$Trise_{sync}$	2	-	6	nS
SYNC fall time	$Tfall_{sync}$	2	-	6	nS
SDATA_IN rise time	$Trise_{din}$	2	-	6	nS
SDATA_IN fall time	$Tfall_{din}$	2	-	6	nS
SDATA_OUT rise time	$Trise_{dout}$	2	-	6	nS
SDATA_OUT fall time	$Tfall_{dout}$	2	-	6	nS

9.2.5. AC-link Low Power Mode Timing



Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	uS

9.2.6. ATE Test Mode



Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	T_{off}	15.0	-	-	nS
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	nS

Notes:

1. All AC-link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the trailing edge of RESET# causes AC '97's AC-link outputs to go high impedance which is suitable for ATE in circuit testing.

2. A vendor specific internal test mode can be entered by bringing SYNC high for the trailing edge of RESET#. This mode has no effect on AC '97 AC-link output signal levels.

3. Once either of the two test modes have been entered, AC '97 must be issued another RESET# with all AC-link signals low to return to the normal operating mode.

10. Analog Performance Characteristics

(Standard test conditions unless otherwise noted: $T_{ambient}$ = 25^{0}C, AVdd = DVdd = 5.0 V +/- 5%; Input Voltage Levels: Logic Low = 0.8V, Logic High = 2.4V; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0dB = 1Vrms, 10KΩ/50pF load, Testbench Characterization BW: 20 Hz - 20KHz, 0dB attenuation; tone and 3D disabled)

Parameter	Min	Typ	Max	Units
Full Scale Input Voltage:				
Line Inputs	-	1.0	-	
Mic Inputs[1]	-	0.1	-	
Full Scale Output Voltage:	-	-	-	
Line Output	-	1.0	-	Vrms
Headphone Output	-	-	1.41	
Analog S/N:				
CD to LINE_OUT	90	-	-	dB
Other to LINE_OUT	-	85	-	
Analog Frequency Response[2]	20	-	20,000	Hz
Digital S/N[3]				
D/A	85	90	-	dB
A/D	75	80	-	
Total Harmonic Distortion:				
Line Output[4]	-	-	0.02	%
Headphone Output[5]	-	-	1.0	
D/A & A/D Frequency Response[6]	20	-	19,200	Hz
Transistion Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection[7]	-74	-	-	dB
Out-of-Band Rejection[8]	-	-40	-	dB
Group Delay	-	-	1	mS
Power Supply Rejection Ratio (1KHz)	-	-40	-	dB
Crosstalk between Inputs channels	-	-	-70	dB
Spurious Tone Reduction	-	-100	-	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Input Impedance	10	-	-	KOhm
Input Capacitance	-	15	-	pF
Vrefout	-	2.25-2.75	-	V

Notes:

(1) With +20dB Boost on, 1.0Vrms with Boost off

(2) ±1dB limits

(3) The ratio of the rms output level with 1KHz full scale input to the rms output level with all zeros into the digital input. Measured "A wtd" over a 20Hz to a 20KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).

(4) 0 dB gain, 20 KHz BW, 48 KHz Sample Frequency

(5) +3dB output into 32Ω load

(6) ±0.25dB limits

(7) Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.

(8) The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback,

over a bandwidth 28.8 to 100 KHz, with respect to a 1VRMS DAC output.